WHAT IS CLAIMED IS:

1. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a semiconductor thin film formed on an insulating substrate and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.

2. A static random access memory according to claim 1, wherein said semiconductor thin film is formed of polysilicon.

3. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a gate electrode formed on an insulating substrate and a semiconductor thin film formed on said gate electrode via a gate

insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just over the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with sad channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.

4. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising an insulating film formed on a semiconductor substrate, a semiconductor thin film formed on said insulating layer and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.